REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Update drawing to current requirements. - drw	02-04-25	Raymond Monnin

THE FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

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REV STATUS	REV	A	A	A	A	A	A	A	A	A	A	A			
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11			

PMIC N/A

PREPARED BY
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DRAWING APPROVAL DATE
90-01-24

REVISION LEVEL
A

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216
http://www.dscc.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUIT, LINEAR, OCTAL, VOLTAGE MODE, 8-BIT D/A CONVERTER, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-88663**

SHEET 1 OF 11

DSCC FORM 2233
APR 97

5962-E317-02

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

5962-88663	01	L	A
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device types. The device types identify the circuit function as follows:

Device type	Generic number	Circuit function	Total unadjusted error
01	7228T	Octal, CMOS, 8-bit voltage-mode DAC	±2.0 LSB
02	7228U	Octal, CMOS, 8-bit voltage-mode DAC	±1.0 LSB

1.2.2 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
L	GDIP3-T24 or CDIP4-T24	24	dual-in-line
3	CQCC1-N28	28	square leadless chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

V_{DD} to ground range ..... -0.3 V dc to +17 V dc
V_{DD} to V_{SS} range ..... +0.3 V dc to +24 V dc
Digital input voltage to ground range ..... -0.3 V dc to V_{DD}
V_{REF} to ground range ..... -0.3 V dc to V_{DD}
V_{OUT} to ground range 1/ ..... V_{SS} to V_{DD}
Storage temperature range ..... -65°C to +150°C
Lead temperature (soldering, 10 seconds) ..... +300°C
Power dissipation (P_D) ..... 1.0 W 2/
Thermal resistance, junction-to-case (θ_{JC}) ..... See MIL-STD-1835
Junction temperature (T_J) ..... +175°C

1.4 Recommended operating conditions.

Operating voltage range for dual supply:
  Positive supply range (V_{DD}) ..... +10.8 V dc to +16.5 V dc
  Negative supply range (V_{SS}) ..... -4.5 V dc to -5.5 V dc
  Reference voltage range (V_{REF}) ..... +2.0 V dc to +10.0 V dc
Operating voltage range for dual supply:
  Positive supply range (V_{DD}) ..... +13.5 V dc to +16.5 V dc
  Negative supply range (V_{SS}) ..... 0 V dc
  Reference voltage range (V_{REF}) ..... +10 V dc
Ambient operating temperature range (T_A) ..... -55°C to +125°C

1/ Outputs may be shorted to any voltage in the range V_{SS} to V_{DD} provided that the power dissipation is not exceeded. Typical short circuit current for a short to ground or V_{SS} is 50 mA.
2/ Derate above T_A = +75°C at 2.0 mW/°C.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103 (see 6.6 herein). For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required in accordance with MIL-PRF-38535, appendix A.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

c. Subgroup 12 test is used for grading and part selection at T_A = +25°C and is not included in PDA calculations.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Total unadjusted error 2/	TUE1	V_{DD} = 15 V ±10%, V_{REF} = +10 V, single supply only	1, 2, 3	01		±2.0	LSB
			1	02		±2.0	
			2, 3, 12			±1.0	
Total unadjusted error 2/, 3/	TUE2	V_{REF} = +10 V, dual supply only	1, 2, 3	01		±2.0	LSB
			1	02		±2.0	
			2, 3, 12			±1.0	
Relative accuracy	RA		1, 2, 3	01		±1.0	LSB
			1	02		±1.0	
			2, 3, 12			±0.5	
Differential nonlinearity	DNL1	Guaranteed monotonic, single supply only	1, 2, 3	All		±1.0	LSB
Differential nonlinearity 3/	DNL2	Dual supply only	1, 2, 3	All		±1.0	LSB
Full scale error 4/	FSE		1, 2, 3	01		±1.0	LSB
			1	02		±1.0	
			2, 3, 12			±0.5	
Zero code error	ZCE		1	All		±25	mV
			2, 3	01		±30	
				02		±20	
			12	02		±15	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Load resistance	R_L	V_{OUT} = ±10 V, dual and single supply	1, 2, 3	All	2.0		kΩ
Reference input voltage range	V_{REF}		1, 2, 3	All	2.0	10	V
Reference resistance	R_{IN}	Dual supply only	1, 2, 3	All	2.0		kΩ
Reference input capacitance 5/	C_{IN} (REF)	Dual and single supply, T_A = +25°C	4	All		500	pF
Digital input high voltage	V_{INH}	Dual supply only, input coding binary	1, 2, 3	All	2.4		V
Digital input low voltage	V_{INL}	Dual supply only, input coding binary	1, 2, 3	All		0.8	V
Digital input leakage current	I_{ILC}	Dual supply only, input coding binary	1, 2, 3	All		±1.0	µA
Digital input capacitance	C_{IN}	Dual supply only, T_A = +25°C	4	All		8	pF
Functional tests		See 4.3.1d	7	All			
Voltage output slew rate 3/	SR	Dual and single supply	9, 10, 11	All	2		V/µs
Voltage output settling time 3/, 6/	t_{SL}	Positive full scale change, dual and single supply, V_{REF} = +10 V	9, 10, 11	All		5.0	µs
		Negative full scale change, V_{REF} = +10 V — Dual supply				5.0	
		Negative full scale change, V_{REF} = +10 V — Single supply				7.0	
Power supply current	I_{DD}		1	All		16	mA
			2, 3			22	
	I_{SS}	Dual supply only	1			-14	
			2, 3			-20	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Address to $\overline{WR}$ setup time 3/	t_1	Dual and single supply, see figure 3 7/	9, 10, 11	All	0		ns
Address to $\overline{WR}$ hold time 3/	t_2	Dual and single supply, see figure 3 7/	9, 10, 11	All	0		ns
Data valid to $\overline{WR}$ setup time 3/	t_3	Dual and single supply, see figure 3 7/	9	All	70		ns
			10, 11		100		
Data valid to $\overline{WR}$ hold time 3/	t_4	Dual and single supply, see figure 3 7/	9, 10, 11	All	10		ns
Write pulse width 3/	t_5	Dual and single supply, see figure 3 7/	9	All	95		ns
			10, 11		150		

1/ Measurements apply with dual supplies, $R_L = 2.0\ k\Omega$, and $C_L = 100$ pF, unless otherwise specified. Refer to 1.4 for conditions of dual and single supplies.

2/ Includes zero code error, relative accuracy, and full scale error.

3/ If not tested, shall be guaranteed to the limits specified in table I.

4/ Calculated after zero code error has been adjusted out.

5/ Occurs when each DAC is loaded with all logic 1's.

6/ Settling time to ±0.5 LSB with $V_{REF} = +10$ V.

7/ All input rise and fall times measured from 10 percent to 90 percent, $t_r = t_f = 5.0$ ns. Timing measurement reference level is $\frac{V_{INH} + V_{INL}}{2}$.

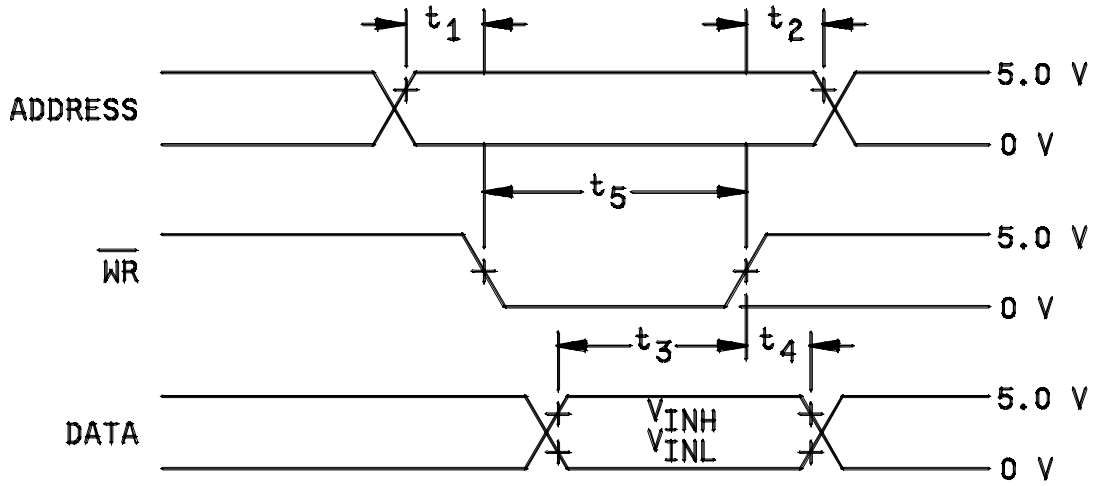
Device types	All	
Case outlines	L	3
Terminal number	Terminal symbol	
1	V_{DD}	NC
2	V_{OUT8}	V_{DD}
3	V_{OUT7}	V_{OUT8}
4	V_{OUT6}	V_{OUT7}
5	V_{OUT5}	V_{OUT6}
6	V_{OUT4}	V_{OUT5}
7	V_{OUT3}	V_{OUT4}
8	V_{OUT2}	NC
9	V_{OUT1}	V_{OUT3}
10	V_{SS}	V_{OUT2}
11	V_{REF}	V_{OUT1}
12	GROUND	V_{SS}
13	DB7 (MSB)	V_{REF}
14	DB6	GROUND
15	DB5	NC
16	DB4	DB7 (MSB)
17	DB3	DB6
18	DB2	DB5
19	DB1	DB4
20	DB0 (LSB)	DB3
21	$\overline{WR}$	DB2
22	A2	NC
23	A1	DB1
24	A0	DB0 (LSB)
25	- - -	$\overline{WR}$
26	- - -	A2
27	- - -	A1
28	- - -	A0

FIGURE 1. Terminal connections.

Control inputs				Operation
$\overline{WR}$	A2	A1	A0	
H	X	X	X	No operation, device not selected
L	L	L	L	DAC1 transparent
_Γ	L	L	L	DAC1 latched
L	L	L	H	DAC2 transparent
L	L	H	L	DAC3 transparent
L	L	H	H	DAC4 transparent
L	H	L	L	DAC5 transparent
L	H	L	H	DAC6 transparent
L	H	H	L	DAC7 transparent
L	H	H	H	DAC8 transparent

H = High state, L = Low state, X = Don't care, _Γ = Low to High transition

FIGURE 2. Truth table.



NOTE: The selected input latch is transparent while $\overline{WR}$ is low, thus invalid data during this time can cause spurious ouputs.

FIGURE 3. Write cycle timing diagram.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 12
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 9**, 10**, 11**, 12
Groups C and D end-point electrical parameters (method 5005)	1, 12

* PDA applies to subgroup 1.
** Subgroups 9, 10, and 11, if not tested, shall be guaranteed to the limits specified in table I.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5, 6, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and $C_{IN(REF)}$ measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance. Sample size is 5 devices with zero failures allowed.

d. Subgroups 7 shall include verification of the truth table.

e. Subgroup 12 test is used for grading and part selection at T_A = +25°C

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 02-04-25

Approved sources of supply for SMD 5962-88663 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-88663013A	24355	AD7228TE/883B
5962-8866301LA	3/	AD7228TQ/883B
5962-88663023A	24355	AD7228UE/883B
5962-8866302LA	24355	AD7228UQ/883B

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source.

Vendor CAGE number	Vendor name and address
24355	Analog Devices Rt 1 Industrial Park PO Box 9106 Point of contact: Norwood, MA 02062 804 Woburn Street Wilmington, MA 01887-3462